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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,101	01/28/2004	Chul Woo Park	AMKOR-100A	2186

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,101	PARK ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,8-12,16 and 18-20* is/are rejected.

7)☒ Claim(s) *3-5,7,13-15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment and Response filed June 08, 2006. The Examiner acknowledges the amendment to Claim 1 and the addition of new Claim 20. Claims 1-20 are now pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Osako et al. (US 6,988,668 B2) Lo et al. (US 5,617,297)†

Maeda et al. (US 6,433,285 B2)

†Already made of record in Examiner's previous Office Action of March 07, 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 11, 12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Osako et al.

As to Claim 1, Osako et al. discloses, in Figs. 1 and 2, a memory card 1 (col.4: 62-67) comprising: a substrate 5 having opposed top and bottom surfaces and a plurality of terminals 6 disposed on the bottom surface thereof; at least one component 7 mounted to the top surface of the substrate 5 and electrically connected to the terminals 6 thereof (col.5: 54-61); a first encapsulation part 3 formed on the bottom surface of the substrate 5; and a second encapsulation part 8 formed on the top surface of the substrate 5 and encapsulating the component 7 mounted thereto, the second encapsulation part 8 being separate from the first encapsulation part 3 (Figs. 18-21).

As to Claim 2, Osako et al. further discloses the first encapsulation part 3 is formed to include an opening therein, the terminals 6 of the substrate being exposed in the opening (Fig. 1; col.6: 13-16).

As to Claim 11, Osako et al. discloses method for fabricating a memory card comprising the steps of: a) providing a substrate 5 having opposed top and bottom surfaces and a plurality of terminals 6 disposed on the bottom surface thereof (Fig. 6); b) forming a first encapsulation part 3 on the bottom surface of the substrate 5 (Figs. 19-21); c) mounting at least one component 7 to the top surface of substrate 5 in a manner wherein the component 7 is electrically connected to the terminals 6 (Fig. 21; col.5: 54-61); and d) forming a second encapsulation part 8 on the top surface of the substrate 5 in a manner encapsulating the component 7 mounted thereto (Figs. 8 and 9).

As to Claim 12, Osako et al. further discloses forming first encapsulation part 3 to include an opening therein, the terminals 6 of the substrate 5 being exposed in the opening (Figs. 1 and 19-21; col.6: 13-16).

As to Claim 20, Osako et al. discloses a method for fabricating a memory card comprising the steps of: a) providing a substrate 5 having opposed top and bottom surfaces and a plurality of terminals 6 disposed on the bottom surface thereof (Fig. 6); b) applying a mold compound 3 to the bottom surface of the substrate 5 (Figs. 19-21); c) mounting at least one component 7 to the top surface of the substrate 5 in a manner wherein the component 7 is electrically connected to the terminals 6 (Fig. 21; col.5: 54-61); and d) applying a mold compound 8 to the top surface of the substrate 5 in a manner encapsulating the component 7 mounted thereto (Figs. 8 and 9).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 6, 8, 9, 11, 16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. in view of Osako et al.

A) As to Claim 1:

I. Maeda et al. discloses, in Figs. 1a,b and 2 (embodiment 1) and Fig. 7 (embodiment 3, common to embodiment 1 except for components being mounted on both top and bottom surfaces of the substrate) an IC card (card 10 in Fig. 1a,b and 2; card 70 in Fig. 7) comprising: a substrate 11--hereinafter referenced as "17," as in Fig. 2, "17" being the base portion of substrate 11 on which component pads 19 and wiring 20 is fabricated) [*Examiner's Note*: substrate 17 is misnumbered as "71" in Fig. 7]--having opposed top and bottom surfaces and a plurality of terminals 18 disposed on the bottom surface thereof; at least one component 13 mounted to the top surface of the substrate (i.e., the surface opposite the terminal-carrying bottom surface, as seen in Fig. 7, "top" and "bottom" being terms relative to arbitrary spatial orientation of the substrate) and electrically connected to the terminals 18 thereof (col.8: 65-col.9: 6); a first encapsulation part 16 formed on the "bottom" (upper) surface of substrate 17 (Fig. 7); and a second encapsulation part 16 formed on the "top" (lower) surface of substrate 17 (Fig. 7) and encapsulating the component 13 mounted thereto, the second encapsulation part 16 being separate from the first encapsulation part 16 (Fig. 7).

II. Maeda et al. does not teach the IC card function (e.g., a memory card).

III. Osako et al., in the same field of endeavor teaches the IC card configured as a memory card (col.4: 62-67).

IV. Since both Maeda et al. and Osako et al. are both in the same field of endeavor manufacturing IC cards with at least one semiconductor device mounted thereon, then the use of semiconductor memory devices and card circuit configuration for forming the memory card in Osako et al. would have been readily recognized as an application for the semiconductor IC card in the pertinent art of Maeda et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the card circuitry and use semiconductor memory devices in the IC card of Maeda et al. to form a memory card for electronic applications, as taught by Osako et al.

B) As to Claim 6, modified Maeda et al. further discloses, in Fig. 7, the first encapsulation part 16 and the second encapsulation part 16 are each fabricated from an epoxy mold compound (col.6: 15-17).

C) As to Claim 8, modified Maeda et al. further discloses multiple components 13 mounted to the top surface (lower surface of substrate 17 in Fig. 7) and electrically connected to the terminals 18 thereof (col.8: 65-col.9: 6).

D) As to Claim 9, modified Maeda et al. further discloses the semiconductor component devices 13 are each a semiconductor die (unpackaged and wire-bonded to substrate 17), as depicted in Figs. 2 and 7 (col.8: 52-56).

E) As to Claim 11:

I. Maeda et al. discloses, in Figs. 1a,b and 2 (embodiment 1) and Fig. 7 (embodiment 3, common to embodiment 1 except for components being mounted on both top and bottom surfaces of the substrate) a method for fabricating an IC card (card

10 in Fig. 1a,b and 2; card 70 in Fig. 7) comprising: a) providing a substrate 11--hereinafter referenced as "17," as in Fig. 2, "17" being the base portion of substrate 11 on which component pads 19, 20 and wiring 12 is fabricated) [*Examiner's Note*: substrate 17 is misnumbered as "71" in Fig. 7]--having opposed top and bottom surfaces and a plurality of terminals 18 disposed on the bottom surface thereof ("top" and "bottom" being terms relative to arbitrary spatial orientation of the substrate, the "top" being the lower surface of substrate 17 in Fig. 7 and the "bottom" being the upper surface of substrate 17 in Fig. 7); b) forming a first encapsulation part 16 formed on the "bottom" (upper) surface of substrate 17 (i.e., the surface of substrate 17 bearing the terminals 18 and components 13); c) mounting at least one component 13 mounted to the top surface of the substrate (i.e., the lower surface opposite the upper terminal-carrying bottom surface, as seen in Fig. 7) in a manner wherein the component 13 is electrically connected to the terminals 18 (col.8: 65-col.9: 6); and d) forming a second encapsulation part 16 formed on the "top" (lower) surface of substrate 17 and encapsulating the component 13 mounted thereto (Fig. 7).

II. Maeda et al. does not teach the IC card function (e.g., a memory card).

III. Osako et al., in the same field of endeavor teaches the IC card configured as a memory card (col.4: 62-67).

IV. Since both Maeda et al. and Osako et al. are both in the same field of endeavor manufacturing IC cards with at least one semiconductor device mounted thereon, then the use of semiconductor memory devices and card circuit configuration

for forming the memory card in Osako et al. would have been readily recognized as an application for the semiconductor IC card in the pertinent art of Maeda et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the card circuitry and use semiconductor memory devices in the IC card of Maeda et al. to form a memory card for electronic applications, as taught by Osako et al.

F) As to Claim 16, modified Maeda et al. further discloses, in Fig. 7, steps b) and d) comprise the first encapsulation part 16 and the second encapsulation part 16 are each fabricated from an epoxy mold compound (col.6: 15-17).

G) As to Claim 18, modified Maeda et al. further discloses step c) comprises mounting and electrically connecting a plurality of components 13 to the substrate 17 (Fig. 7; col.5: 15-41; col.8: 65-col.9: 6).

H) As to Claim 19:

I. Modified Maeda et al. discloses that **the bottom surface** of substrate 17 includes **semiconductor die 13 wirebonded on lands 20, passive devices (chip resistors, chip capacitors 15) surface mounted on lands 19** adjacent the semiconductor die 13, and terminals 18, all interconnected by substrate wiring 12 (Fig. 2 and upper surface of Fig. 7). On the top surface of substrate 17 (lower surface of Fig. 7) Maeda et al. discloses only semiconductor die 13 wirebonded on lands 20 interconnected with the above-cited circuitry and components of the bottom surface through conductive vias (col.8: 65-col.9: 6) but does not teach passive devices mounted **on that top surface** (i.e., the lower surface in Fig. 7).

IIa. In one further modification, it would have been an obvious matter of engineering choice to relocate the passive devices 15 (as seen on the bottom surface shown in Figs. 1 and 2, to the corresponding positions on the top surface (the lower surface of Fig. 7) since the electrical distances between the passive devices 15 and semiconductor die 13 would be the same on both sides of substrate 17 by symmetry. Thus, the memory card in Fig. 7 modified to have the passive devices 15 mounted on the top surface (lower surface in Fig. 7) would function identically to the memory card disclosed wherein the passive devices are mounted on the bottom surface (upper surface of Fig. 7, as seen in Figs. 1 and 2) and therefore it would have been an obvious matter of engineering choice to mount the passive devices 15 on the top surface instead of the bottom surface of substrate 17 by virtue of the equivalent electrical performance due to the electrical wiring symmetry on the substrate and also since it is old and well-known in the art that one of ordinary skill in the art would know the application requirements and the particular layout of the IC card wiring and components considered optimal for that electronic application.

IIb. In an alternate further modification, it is noted that Maeda et al. adds the semiconductor die 13 to the top surface (lower surface in Fig. 7) of substrate 17 in order to increase the semiconductor device density of the IC memory card (col.8: 52-62). Accordingly, since the bottom surface (see Figs. 1 and 2 which correspond to the upper surface of Fig. 7) has the passive devices 15 surface mounted thereon in order to perform any of signal filtering, noise decoupling, current limiting, or functional combinations thereof, for the semiconductor die 13 mounted adjacent thereto on the

bottom surface, then it would have been obvious to one of ordinary skill in the art, as a matter of engineering choice to also mount passive devices 15 on the top surface (i.e., the lower surface of Fig. 7) as well, in order to perform the same signal conditioning for the semiconductor die 13 on that side of the substrate in applications that require enhanced signal conditioning for the semiconductor die on both sides of the substrate.

III. Therefore, in view of the modification in either of IIa or IIb, above, it would have been obvious to one of ordinary skill in the art to surface mount the passive devices 15 to the top surface of memory card (i.e., the surface of the card opposite the surface with terminals 18) in Maeda et al. in order to provide signal conditioning for the semiconductor die 13 wirebonded adjacent thereto responsive to the requirements of an electronic application.

I) As to Claim 20:

I. Maeda et al. discloses, in Figs. 1a,b and 2 (embodiment 1) and Fig. 7 (embodiment 3, common to embodiment 1 except for components being mounted on both top and bottom surfaces of the substrate) a method for fabricating an IC card (card 10 in Fig. 1a,b and 2; card 70 in Fig. 7) comprising: a) providing a substrate 11--hereinafter referenced as "17," as in Fig. 2, "17" being the base portion of substrate 11 on which component pads 19 and wiring 20 is fabricated) [*Examiner's Note*: substrate 17 is misnumbered as "71" in Fig. 7]--having opposed top and bottom surfaces and a plurality of terminals 18 disposed on the bottom surface thereof ("top" and "bottom" being terms relative to arbitrary spatial orientation of the substrate, "top" being the lower surface of substrate 17 in Fig. 7 and the "bottom" being the upper surface of substrate

17 in Fig. 7); b) providing a mold compound 16 to the bottom surface of the substrate 17 (i.e., the upper surface of substrate 17 in Fig. 7); c) mounting at least one component 13 to the "top" (lower) surface of substrate 17 in a manner wherein the component 13 is electrically connected to the terminals 18 (col.8: 65-col.9: 6); and d) applying a mold compound 13 to the top surface of substrate 17 in a manner encapsulating the component 13 mounted thereto (Fig. 7).

II. Maeda et al. does not teach the IC card function (e.g., a memory card).

III. Osako et al., in the same field of endeavor teaches the IC card configured as a memory card (col.4: 62-67).

IV. Since both Maeda et al. and Osako et al. are both in the same field of endeavor manufacturing IC cards with at least one semiconductor device mounted thereon, then the use of semiconductor memory devices and card circuit configuration for forming the memory card in Osako et al. would have been readily recognized as an application for the semiconductor IC card in the pertinent art of Maeda et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the card circuitry and use semiconductor memory devices in the IC card of Maeda et al. to form a memory card for electronic applications, as taught by Osako et al.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. in view of Osako et al., as applied to Claim 9 above, and further in view of Lo et al.

I. Modified Maeda et al. discloses that **the bottom surface** of substrate 17 includes **semiconductor die 13 wirebonded on lands 20, passive devices (chip**

resistors, chip capacitors 15) surface mounted on lands 19 adjacent the semiconductor die 13, and terminals 18, all interconnected by substrate wiring 12 (Fig. 2 and upper surface of Fig. 7). On the top surface of substrate 17 (lower surface of Fig. 7) Maeda et al. discloses only semiconductor die 13 wirebonded on lands 20 interconnected with the above-cited circuitry and components of the bottom surface through conductive vias (col.8: 65-col.9: 6) but does not teach passive devices mounted **on that top surface** (i.e., the lower surface in Fig. 7).

IIa. In one further modification, it would have been an obvious matter of engineering choice to relocate the passive devices 15 (as seen on the bottom surface shown in Figs. 1 and 2, to the corresponding positions on the top surface (the lower surface of Fig. 7) since the electrical distances between the passive devices 15 and semiconductor die 13 would be the same on both sides of substrate 17 by symmetry. Thus, the memory card in Fig. 7 modified to have the passive devices 15 mounted on the top surface (lower surface in Fig. 7) would function identically to the memory card disclosed wherein the passive devices are mounted on the bottom surface (upper surface of Fig. 7, as seen in Figs. 1 and 2) and therefore it would have been an obvious matter of engineering choice to mount the passive devices 15 on the top surface instead of the bottom surface of substrate 17 by virtue of the equivalent electrical performance due to the electrical wiring symmetry on the substrate and also since it is old and well-known in the art that one of ordinary skill in the art would know the application requirements and the particular layout of the IC card wiring and components considered optimal for that electronic application.

IIb. In an alternate further modification, it is noted that Maeda et al. adds the semiconductor die 13 to the top surface (lower surface in Fig. 7) of substrate 17 in order to increase the semiconductor device density of the IC memory card (col.8: 52-62). Accordingly, since the bottom surface (see Figs. 1 and 2 which correspond to the upper surface of Fig. 7) has the passive devices 15 surface mounted thereon in order to perform any of signal filtering, noise decoupling, current limiting, or functional combinations thereof, for the semiconductor die 13 mounted adjacent thereto on the bottom surface, then it would have been obvious to one of ordinary skill in the art, as a matter of engineering choice to also mount passive devices 15 on the top surface (i.e., the lower surface of Fig. 7) as well, in order to perform the same signal conditioning for the semiconductor die 13 on that side of the substrate in applications that require enhanced signal conditioning for the semiconductor die on both sides of the substrate.

IIc. Therefore, in view of the modification in either of IIa or IIb, above, it would have been obvious to one of ordinary skill in the art to surface mount the passive devices 15 to the top surface of memory card (i.e., the surface of the card opposite the surface with terminals 18) in Maeda et al. in order to provide signal conditioning for the semiconductor die 13 wirebonded adjacent thereto responsive to the requirements of an electronic application.

IIIa. Modified Maeda et al., as further modified in IIa, IIb and IIc, above, does not teach that, the semiconductor devices (col.5: 17-18; col.8: 52-56) encompass a semiconductor package as well as the semiconductor die 13 depicted in Figs. 1, 2 and 7).

IIIb. Lo et al. discloses a memory card having semiconductor devices inclusive of semiconductor die and semiconductor packages (e.g., encapsulated ICs, multichip packages) as well as passive devices, the semiconductor devices and passive devices mounted on both sides of the card substrate, for the purpose of providing a memory card with the functionality required by the application (col.3: 27-67).

IIIc. Since both modified Maeda et al. and Lo et al. are practitioners in the art of IC memory cards, then the surface mounting of a semiconductor package (e.g., an encapsulated IC and/or a multichip package) to either or both sides of the card substrate, in addition to the wirebonded semiconductor die and surface mounted passive devices for the purpose of providing the required functionality for the memory card, as taught by Lo et al., would have been readily recognized in the pertinent memory card art of modified Maeda et al. for achieving the same objective.

IIId. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Maeda et al. by including a surface mounted semiconductor package on the same surface as the surface mounted passive device and wirebonded semiconductor die to enhance the functionality of the memory card of modified Maeda et al. for meeting the requirements of the application, as taught by Lo et al.

Allowable Subject Matter

9. Claims 3-5, 7, 13-15 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments with respect to amended Claim 1, originally filed Claim 11 and new Claim 20, in the Response filed June 08, 2006, have been considered but are moot in view of the new ground(s) of rejection.

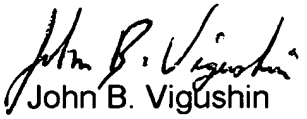
11. New grounds of rejection has been raised by the Examiner for originally filed Claim 11. Therefore, the present Office Action is made NON-FINAL.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
August 17, 2006